
From Lothar Thiele

Site: Phds

Supervised Phd Theses

The following list contains some of the PhD theses that have been supervised by me during my time at the University of Saarland, Saarbruecken and at the ETH Zurich.

1. Juergen Teich: A Compiler for Application-Specific Processor Arrays. PhD Thesis, Institute of Microelectronics, University of Saarland, Saarbruecken, Germany, 1993.
2. Ulrich Arzt: COMPAR – Ein Compiler für massiv parallele Architekturen. PhD Thesis, Institute of Microelectronics, University of Saarland, Saarbruecken, Germany, 1994.
3. Wolfgang Backes: The Structure of Longest Paths in Periodic Graphs. PhD Thesis, Institute of Microelectronics, University of Saarland, Saarbruecken, Germany, 1994. [Postscript](#)
4. Christian Heckler: Automatische Parallelisierung und parallele Gitterbasisreduktion. PhD Thesis, Institute of Microelectronics, University of Saarland, Saarbruecken, Germany, 1995. [Postscript](#)
5. Alexander Bachmann: Systematischer Entwurf heterogener Multiprozessorsysteme. PhD Thesis, Institute of Microelectronics, University of Saarland, Saarbruecken, Germany, 1995. [Postscript](#)
6. Jean-Paul Theis: Parallel Processor Architectures for Image Processing. PhD Thesis, Institute of Microelectronics, University of Saarland, Saarbruecken, Germany, 1996.
7. Joachim Koenig--Baltes: Online-Verfahren der Ganzzahlarithmetik und ihre Realisierung in einem Koprozessor. PhD Thesis, Institute of Microelectronics, University of Saarland, Saarbruecken, Germany, 1996.
8. Lee Zhang: Scheduling and allocation with integer linear programming. PhD Thesis, Institute of Microelectronics, University of Saarland, Saarbruecken, Germany, 1996. [Postscript](#)
9. Tobias Blickle: Theory of evolutionary algorithms and applications to system design. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, 1996. [Postscript](#)
10. Rob Esser: An object oriented approach to embedded system design. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, 1996. [Postscript](#)

11. Martin Gerber: Parallelising Molecular Dynamics for Message Passing Systems. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, November 1999. [Postscript](#)
12. Eckart Zitzler: Evolutionary Algorithms for Multiobjective Optimization: Methods and Applications. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, December 1999. [Postscript](#)
13. Martin Naedele: On the Modeling and Evaluation of Real-Time Systems. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, March 2000. [Postscript](#)
14. Karsten Strehl: Symbolic Methods Applied to Formal Verification and Synthesis in Embedded Systems Design. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, March 2000. [Postscript](#)
15. Joern Janneck: Syntax and semantics of graphs – An approach to the specification of visual notations for discrete-event systems. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, June 2000. [Postscript](#)
16. Matthias Gries: Algorithm-Architecture Trade-offs in Network Processor Design. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, July 2001. [Postscript pdf](#)
17. Michael Eisenring: Communication Channel Synthesis for Heterogeneous Embedded Systems. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, Oktober 2002. [pdf](#)
18. Ferdinand Gramsamer: Scalable Flow Control for Interconnection Networks. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, March 2003. [pdf](#)
19. Samarjit Chakraborty: System-Level Timing Analysis and Scheduling for Embedded Packet Processors. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, April 2003. [pdf](#)
20. Marco Laumanns: Analysis and Applications of Evolutionary Multiobjective Optimization Algorithms. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, August 2003. [pdf](#)
21. Philipp Kutter: Montages – Engineering of Computer Languages. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, 2004. [Postscript pdf](#)
22. Andreas Hubert Moglestue: CIP Model Checking. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, 2004. [pdf](#)
23. Philipp Blum: Guaranteed Time Synchronization in Wireless and Ad-Hoc Networks. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, March 2005. [pdf](#)
24. Herbert Walder: Operating System Design for Partially Reconfigurable Logic Devices. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, April 2005. [pdf](#)

25. Jan Beutel: Design and Deployment of Wireless Networked Embedded Systems. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, August 2005. pdf
26. Gero Dittmann: On Instruction-Set Generation for Specialized Processors. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, August 2005. pdf
27. Alexander Maxiaguine: Modeling Multimedia Workloads for embedded system design. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, October 2005. pdf
28. Lennart Meier: Interval-Based Time Synchronization for Mobile Ad-Hoc Networks. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, December 2005. pdf
29. Jonas Greutert: Abstraction and Implementation of Predictable Packet Processing Systems. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, February 2006. pdf
30. Simon Kuenzli: Efficient Design Space Exploration for Embedded Systems. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, April 2006. pdf
31. Christian Plessl: Hardware Virtualization on a Coarse-grained Reconfigurable Processor. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, July 2006. pdf
32. Ernesto Wandeler: Modular Performance Analysis and Interface-Based Design for Embedded Real-Time Systems. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, September 2006. pdf
33. René Beutler: Improving Speech Recognition through Linguistic Knowledge. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, January, 2007. pdf
34. Matthias Dyer: Distributed Embedded Systems - Validation Strategies. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, April, 2007. pdf
35. Harald Romsdorfer: Polyglot Text-to-Speech Synthesis - Text Analysis and Prosody Control. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, January 2009. pdf
36. Clemens Moser: Power Management in Energy Harvesting Embedded Systems. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, March 2009. pdf
37. Andreas Meier: Safety-Critical Wireless Sensor Networks. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, June, 2009. pdf
38. Tobias Kaufmann: A Rule-based Language Model for Speech Recognition. PhD Thesis, Computer Engineering and Networks Laboratory, ETH Zurich, Switzerland, October 2009. postscript

Retrieved from <http://www.tik.ee.ethz.ch/~thiele/pmwiki/pmwiki.php/Site/Phds>
Page last modified on December 26, 2009, at 06:40 PM

Peer Reviewed Publications (- 2008, part of 2009)

Scientific Journals

- [1] L Thiele, K Miettinen, PJ Korhonen, J Molina. **A Preference-Based Evolutionary Algorithm for Multi-Objective Optimization.** Evolutionary Computation, Vol. 17, No. 3, Pages 411-436, 2009.
- [2] Clemens Moser, Lothar Thiele, Davide Brunelli and Luca Benini. **Adaptive Power Management for Environmentally Powered Systems.** Accepted for publication in IEEE Transactions on Computers, 2009, regular papers.
- [3] Davide Brunelli, Clemens Moser, Lothar Thiele and Luca Benini. **Design of a Solar Harvesting Circuit for Battery-less Embedded Systems.** Accepted for publication in IEEE Transactions on Circuits and Systems I, 2009, regular papers.
- [4] Eckart Zitzler, Lothar Thiele, Johannes Bader: **On Set-Based Multiobjective Optimization.** IEEE Trans. Evolutionary Computation, accepted 2008.
- [5] Lothar Thiele, Kaisa Miettinen, Pekka J. Korhonen, Julian Molina: **A Preference-based Evolutionary Algorithm for Multiobjective Optimization.** Evolutionary Computation, MIT Press, accepted 2008.
- [6] Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: **Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems.** Design Automation for Embedded Systems, Springer Science+Business Media, LLC, accepted 2008.
- [7] Karl Aberer, Gustavo Alonso, Guillermo Barrenetxea, Jan Beutel, Jacques Bovay, Henri Dubois-Ferriere, Donald Kossmann, Marc Parlange, Lothar Thiele, Martin Vetterli: **Infrastructures for a Smart Earth - The Swiss NCCR-MICS initiative.** Praxis der Informationsverarbeitung und Kommunikation, K.G. Saur Verlag, Munich, Germany, Vol. 30, No. 1, pages 20-25, January, 2007.
- [8] Clemens Moser, Davide Brunelli, Lothar Thiele, Luca Benini: **Real-Time Scheduling for Energy Harvesting Sensor Nodes.** Real-Time Systems Journal, Springer Science+Business Media, Netherlands, Vol. 37, No. 3. pages 223-260, 2007.
- [9] Ernesto Wandeler, Lothar Thiele: **Workload correlations in multi-processor hard real-time systems.** Journal of Computer and System Sciences, Vol. 73, No. 2, pages 207-224, 2007.
- [10] Ernesto Wandeler, Lothar Thiele, Marcel Verhoef, Paul Lieveise: **System Architecture Evaluation Using Modular Performance Analysis - A Case Study** Software Tools for Technology Transfer (STTT), Springer, Vol. 8, No. 6, pages 649 - 667, October, 2006.

- [11] Amela Prelic, Stefan Bleuler, Philip Zimmermann, Anja Wille, Peter Bühlmann, Wilhelm Gruissem, Lars Hennig, Lothar Thiele, Eckart Zitzler: **Comparison of Biclustering Methods: A Systematic Comparison and Evaluation of Biclustering Methods for Gene Expression Data.**
Bioinformatics, Oxford University Press, Vol. 22, No. 9, pages 1122-1129, May, 2006.
- [12] Marco Laumanns, Lothar Thiele, Eckart Zitzler: **An efficient, adaptive parameter variation scheme for metaheuristics based on the epsilon-constraint method.**
European Journal of Operational Research, Elsevier, Vol. 169, No. 3, pages 932-942, March, 2006.
- [13] Lothar Thiele, Ernesto Wandeler, Samarjit Chakraborty: **A Stream-Oriented Component Model for Performance Analysis of Multiprocessor DSPs.**
IEEE Signal Processing Magazine, special Issue on Hardware/Software Co-design for DSP, IEEE, Vol. 22, No. 3, pages 38--46, May, 2005.
- [14] Simon Künzli, Lothar Thiele, Eckart Zitzler: **Modular Design Space Exploration Framework for Embedded Systems.**
IEE Proceedings Computers & Digital Techniques, Vol. 152, No. 2, pages 183-192, March, 2005.
- [15] Ernesto Wandeler, Alexandre Maxiaguine, Lothar Thiele: **Quantitative characterization of Event Streams in Analysis of Hard Real-Time Applications.**
Real-time Systems, Springer Science+Business Media B.V., Vol. 29, No. 2, pages 205--225, March, 2005.
- [16] Alexandre Maxiaguine, Samarjit Chakraborty, Simon Künzli, Lothar Thiele: **Evaluating Schedulers for Multimedia Processing on Buffer-Constrained SoC Platforms.**
IEEE Design & Test, IEEE Computer Society Press, Vol. 21, No. 5, pages 368-377, September, 2004.
- [17] Lothar Thiele, Reinhard Wilhelm: **Design for Timing Predictability.**
Real-Time Systems, Vol. 28, No. 2, pages 157-177, 2004.
- [18] Anja Wille, Philip Zimmermann, Eva Vranova, Andreas Fürholz, Oliver Laule, Stefan Bleuler, Lars Hennig, Amela Prelic, Peter von Rohr, Lothar Thiele, Eckart Zitzler, Wilhelm Gruissem, Peter Bühlmann: **Sparse graphical Gaussian modeling of the isoprenoid gene network in Arabidopsis thaliana.**
Genome Biology, Vol. 5, No. 11, pages R92, 2004.
- [19] Urs Anliker, Jan Beutel, Matthias Dyer, Rolf Enzler, Paul Lukowicz, Lothar Thiele, Gerhard Tröster: **A Systematic Approach to the Design of Distributed Wearable Systems.**
IEEE Transactions on Computers, IEEE CS Press, Los Alamitos, CA, Vol. 53, No. 8, pages 1017-1033, August, 2004.
- [20] Marco Laumanns, Lothar Thiele, Eckart Zitzler: **Running Time Analysis of Multiobjective Evolutionary Algorithms on Pseudo-Boolean Functions.**
IEEE Transactions on Evolutionary Computation, Vol. 8, No. 2, pages 170—182, April, 2004.
- [21] Marco Laumanns, Lothar Thiele, Eckart Zitzler: **Running Time Analysis of Evolutionary Algorithms on a Simplified Multiobjective Knapsack Problem.**
Natural Computing, Vol. 3, No. 1, pages 37—51, 2004.
- [22] Samarjit Chakraborty, Simon Künzli, Lothar Thiele, Andreas Herkersdorf, Patricia Sagmeister: **Performance Evaluation of Network Processor Architectures: Combining Simulation with Analytical Estimation.**
Computer Networks, Vol. 41, No. 5, pages 641--665, 2003.

- [23] Christian Plessl, Rolf Enzler, Herbert Walder, Jan Beutel, Marco Platzner, Lothar Thiele, Gerhard Tröster: **The case for reconfigurable hardware in wearable computing.** Personal and Ubiquitous Computing, Springer-Verlag, Vol. 7, No. 5, pages 299-308, Oktober, 2003.
- [24] Marco Laumanns, Lothar Thiele, Kalyanmoy Deb, Eckart Zitzler: **Combining Convergence and Diversity in Evolutionary Multi-objective Optimization.** Evolutionary Computation, MIT Press, Vol. 10, No. 3, pages 263-282, 2002.
- [25] Eckart Zitzler, Marco Laumanns, Lothar Thiele, Carlos M. Fonseca, Viviane Grunert da Fonseca: **Performance Assessment of Multiobjective Optimizers: An Analysis and Review.** IEEE Transactions on Evolutionary Computation, Vol. 7, No. 2, pages 117-132, 2003.
- [26] Lothar Thiele, Samarjit Chakraborty, Matthias Gries, Simon Künzli: **Design Space Exploration of Network Processor Architectures.** Network Processor Design: Issues and Practices, Volume 1, Morgan Kaufmann Publishers, pages 55-89, 2002.
- [27] Dirk Ziegenbein, K Richter, Rolf Ernst, Lothar Thiele, Juergen Teich: **SPI - A system model for heterogeneously specified embedded systems.** IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 4, pages 379-389, August 2002.
- [28] Matthias Anlauff, Samarjit Chakraborty, Philipp W. Kutter, Alfonso Pierantonio, Lothar Thiele: **Generating an Action Notation Environment from Montages Descriptions.** International Journal on Software Tools for Technology Transfer (STTT), Springer-Verlag, Vol. 3, No. 4, pages 431--455, 2001.
- [29] Karsten Strehl, Lothar Thiele, Matthias Gries, Dirk Ziegenbein, Rolf Ernst, Juergen Teich: **FunState - An Internal Design Representation for Codesign.** IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 9, No. 4, pages 524-544, August, 2001.
- [30] Michael Eisenring, Lothar Thiele, Eckart Zitzler: **Handling Conflicting Criteria in Embedded System Design.** IEEE Design & Test of Computers, IEEE, Vol. 17, No. 2, pages 51-59, April, 2000.
- [31] Uwe Schwiegelshohn, Lothar Thiele: **Properties of Change Diagrams.** to appear in: In A. Yakovlev, L. Gomes, and L. Lavagno, editors, Hardware Design and Petri Nets, Kluwer Academic Publishers, pages 77-92, March, 2000.
- [32] Lothar Thiele, Juergen Teich, Karsten Strehl: **Regular State Machines.** Journal of Parallel Algorithms and Applications, Vol. 14, No. 8, pages 1-36, August, 2000.
- [33] Eckart Zitzler, Kalyanmoy Deb, Lothar Thiele: **Comparison of Multiobjective Evolutionary Algorithms: Empirical Results.** Evolutionary Computation, MIT Press, Vol. 8, No. 2, pages 173-195, April, 2000.
- [34] Karsten Strehl, Lothar Thiele: **Interval Diagrams for Efficient Symbolic Verification of Process Networks.** IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 19, No. 8, pages 939-956, August, 2000.
- [35] Manfred Morari, Lothar Thiele: **Eingebettete Systeme.** Bulletin of the ETHZ, Vol. 278, pages 18-21, September, 2000.
- [36] Uwe Schwiegelshohn, Lothar Thiele: **Dynamic Min-Max Problems.** Discrete Event Dynamic Systems, Vol. 9, No. 2, pages 111-134, May, 1999.

- [37] Eckart Zitzler, Lothar Thiele: **Multiobjective Evolutionary Algorithms: A Comparative Case Study and the Strength Pareto Approach.**
IEEE Transactions on Evolutionary Computation, Vol. 3, No. 4, pages 257-271, November, 1999.
- [38] Rob Esser, Juergen Teich, Lothar Thiele: **CodeSign: An Embedded System Design Environment.**
Journal Proc of the IEE, Computers and Digital Techniques., pages 171-180, January, 1998.
- [39] Christian Heckler, Lothar Thiele: **Algorithms and complexity for parallel lattice basis reduction.**
SIAM Journal on Computing, Vol. 27, pages 1295-1302, January, 1998.
- [40] Juergen Teich, Tobias Blickle, Lothar Thiele: **System-Level Synthesis Using Evolutionary Algorithms.**
J. Design Automation for Embedded Systems, Vol. 3, pages 23-58, January, 1998.
- [41] Lothar Thiele: **Hardware fuer die visuelle Kommunikation - ein virtuelles Streitgesprach.**
Bulletin of the ETH Zurich (266), September, 1998.
- [42] Juergen Teich, Lothar Thiele, Lee Zhang: **Scheduling of partitioned regular algorithms on processor arrays with constrained resources.**
Int. Journal on VLSI and Signal Processing, Vol. 17, No. 1, pages 5-20, January, 1997.
- [43] Juergen Teich, Shruva Sriram, Lothar Thiele, M Martin: **Performance Analysis of mixed Asynchronous-Synchronous Systems.**
J. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 5, pages 473-484, May, 1997.
- [44] Tobias Blickle, Lothar Thiele: **A Comparison of Selection Schemes Used in Genetic Algorithms.**
Intl. Journal on Evolutionary Computation, Vol. 4, No. 4, January, 1996.
- [45] Joachim König-Baltes, Lothar Thiele: **Algorithm-Architecture Co-Design by Example: A Coprocessor for Seminumerical Algorithms.**
Microprocessors & Microprogramming, Vol. 41, pages 339-357, January, 1995.
- [46] Lothar Thiele: **Scheduling of uniform algorithms with resource constraints.**
Int. Journal VLSI Signal Processing, Int. Journal VLSI Signal Processing, January, 1995.
- [47] Christian Heckler, Lothar Thiele: **Computing Linear Data Dependencies in Nested Loop Programs.**
Parallel Processing Letters (PPL), Vol. 4, No. 4, January, 1994.
- [48] Christian Heckler, Lothar Thiele: **Computing linear data dependencies in nested loop programs.**
Parallel Processing Letters (PPL), Vol. 4, No. 3, pages 193-204, January, 19W94.
- [49] Gerhard Fettweis, Lothar Thiele: **Algebraic recurrence transformations for massive parallelism.**
IEEE Trans. Circuits Systems, December, 1993.
- [50] Juergen Teich, Lothar Thiele: **Partitioning of processor arrays: A piecewise regular approach.**
INTEGRATION: The VLSI Journal, Vol. 14, No. 3, pages 297-332, January, 1993.

- [51] Lothar Thiele, Ulrich Arzt: **On the synthesis of massively parallel architectures.**
International Journal of High Speed Electronics, Vol. 4, No. 2, pages 99-131, January, 1993.
- [52] Lothar Thiele: **Parallel implementation of cellular systems for numerical modelling.**
International Journal of Numerical Modeling, Vol. 5, pages 203-218, January, 1992.
- [53] Juergen Teich, Lothar Thiele: **Control generation in the design of processor arrays..**
Int. Journal on VLSI and Signal Processing, Vol. 3, No. 2, pages 77-92, January, 1991.
- [54] Lothar Thiele: **On the analysis and optimization of selftimed processor arrays..**
INTEGRATION: The VLSI Journal, Vol. 12, No. 2, pages 167-187, January, 1991.
- [55] Juergen Teich, Lothar Thiele: **Systematic design concepts for signal processing arrays (invited paper).**
Frequenz / Journal of telecommunications, Vol. 44, pages 122-132, May, 1990.
- [56] Lothar Thiele, Gerhard Fettweis: **Algorithm transformations for unlimited parallelism (invited paper).**
AEÜ / Electronics and Communications, Vol. 44, No. 2, pages 83-91, March, 1990.
- [57] Uwe Schwiegelshohn, Lothar Thiele: **Linear processor arrays for matrix computations.**
J. on Parallel and Distributed Computing, Vol. 7, pages 28-39, January, 1989.
- [58] Uwe Schwiegelshohn, Lothar Thiele: **A systolic array for the assignment problem.**
IEEE Trans. Computers, pages 1422-1425, November, 1988.
- [59] Uwe Schwiegelshohn, Lothar Thiele: **A systolic array for cyclic-by-rows Jacobi algorithms.**
Journal on Parallel and Distributed Computing, Vol. 4, pages 334-340, January, 1987.
- [60] Lothar Thiele: **An algorithm for rational causal approximation.**
AEÜ / Electronics and Communications, Vol. 4, No. 2, pages 124-128, January, 1986.
- [61] Lothar Thiele: **On the sensitivity of linear state space systems.**
IEEE Trans. Circuits Systems, pages 502--510, January, 1986.
- [62] Lothar Thiele: **An analytic approach to curve fitting.**
AEÜ / Electronics and Communications, Vol. 40, No. 1, pages 51-58, January, 1986.
- [63] Lothar Thiele: **On a special form of the Cauchy-Schwarz inequality.**
Journal of the Francklin Institute, pages 405-412, January, 1985.
- [64] Vedat Tavsanoğlu, Lothar Thiele: **Optimal design of state-space digital filters by simultaneous minimization of sensitivity and round-off noise.**
IEEE Trans. Circuits and Systems, pages 884-888, January, 1984.
- [65] Vedat Tavsanoğlu, Lothar Thiele: **A unifying approach to the design of sensitivity optimal second order state space systems.**
AEÜ / Electronics and Communications, Vol. 38, No. 6, pages 355-362, January, 1984.
- [66] Lothar Thiele: **Design of sensitivity and round-off noise optimal state-space discrete systems.**
Int. Journal of Circuits Theory and Applications, Vol. 12, pages 39-46, January, 1984.

Peer Reviewed Conferences

- [67] Jian-Jia Chen, Andreas Schranzhofer, Lothar Thiele: **Energy Minimization for Periodic Real-Time Tasks on Heterogeneous Processing Units.**
International Parallel and Distributed Processing Symposium (IPDPS), IEEE, Rome Italy, May, 2009.
- [68] Chuan-Yue Yang, Jian-Jia Chen, Tei-Wei Kuo, Lothar Thiele: **An Approximation Scheme for Energy-Efficient Scheduling of Real-Time Tasks in Heterogeneous Multiprocessor Systems.**
ACM/IEEE Conference of Design, Automation, and Test in Europe, ACM/IEEE, Nice, France, April, 2009.
- [69] Nikolay Stoimenov, Simon Perathoner, Lothar Thiele: **Reliable Mode Changes in Real-Time Systems with Fixed Priority or EDF Scheduling.**
Design, Automation and Test in Europe, 2009, DATE '09, Nice, France, April, 2009.
- [70] Jian-Jia Chen, Lothar Thiele: **Energy-Efficient Task Partition for Periodic Real-Time Tasks on Platforms with Dual Processing Elements.**
14th Intl Conference on Parallel and Distributed Systems, IEEE, December, 2008.
- [71] Clemens Moser, Jian-Jia Chen, Lothar Thiele: **Reward Maximization for Embedded Systems with Renewable Energies.**
Embedded and Real-Time Computing Systems and Applications, 2008. RTCSA'08. IEEE Computer Society, Los Alamitos, CA, USA, pages 247-256, August, 2008.
- [72] Andreas F. Meier, Mischa Weise, Jan Beutel, Lothar Thiele: **NoSE: Efficient Initialization of Wireless Sensor Networks.**
6th ACM Conference on Embedded Networked Sensor Systems (SenSys 2008), ACM, Raleigh, North Carolina, USA, November, 2008
- [73] Bengt Jonsson, Simon Perathoner, Lothar Thiele, Wang Yi: **Cyclic Dependencies in Modular Performance Analysis.**
ACM International Conference on Embedded Software (EMSOFT), ACM Press, Atlanta, Georgia, USA, pages 179-188, October, 2008.
- [74] Eckart Zitzler, Lothar Thiele, Johannes Bader: **SPAM: Set Preference Algorithm for Multiobjective Optimization.**
Lecture Notes in Computer Science, Springer, Dortmund, Germany, Vol. 5199, pages 847-858, September, 2008.
- [75] Jian-Jia Chen, Lothar Thiele: **Expected System Energy Consumption Minimization in Leakage-Aware DVS Systems.**
International Symposium on Low Power Electronics and Design, August, 2008.
- [76] Andreas F. Meier, Tobias Rein, Jan Beutel, Lothar Thiele: **Coping with Unreliable Channels: Efficient Link Estimation for Low-Power Wireless Sensor Networks.**
Proc. 5th Intl. Conf. Networked Sensing Systems (INSS 2008), Kanazawa, Japan, June, 2008.
- [77] Matthias Woehrle, Christian Plessl, Roman Lim, Jan Beutel, Lothar Thiele: **EvAnT: Analysis and Checking of event traces for Wireless Sensor Networks.**
Proc. of the IEEE Intl. Conf. on Sensor Networks, Ubiquitous, and Trustworthy Computing, IEEE, June, 2008.
- [78] Kai Huang, Iuliana Bacivarov, Fabian Hugelshofer, Lothar Thiele: **Scalably distributed SystemC simulation for embedded applications.**
International Symposium on Industrial Embedded Systems, pages 271 - 274 , June, 2008.

- [79] Clemens Moser, Lothar Thiele, Davide Brunelli, Luca Benini: **Approximate Control Design for Solar Driven Sensor Nodes.**
Hybrid Systems: Computation and Control, Lecture Notes in Computer Science, Springer , Berlin / Heidelberg, Vol. 4981, pages 634-637, April, 2008.
- [80] Davide Brunelli, Luca Benini, Clemens Moser, Lothar Thiele: **An Efficient Solar Energy Harvester for Wireless Sensor Nodes.**
Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.
- [81] Clemens Moser, Lothar Thiele, Davide Brunelli, Luca Benini: **Robust and Low Complexity Rate Control for Solar Powered Sensors**
Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.
- [82] Samarjit Chakraborty, Tulika Mitra, Abhik Roychoudhury, Lothar Thiele, Unmesh D. Bordoloi, Cem Derdiyok: **Cache-Aware Timing Analysis of Streaming Applications.**
19th Euromicro Conference on Real-Time Systems (ECRTS), Pisa, Italy, pages 159 - 168, July, 2007.
- [83] Linh Phan, Samarjit Chakraborty, P. S. Thiagarajan, Lothar Thiele: **Composing Functional and State-based Performance Models for Analyzing Heterogeneous Real-Time Systems.**
28th IEEE Real-Time Systems Symposium (RTSS), Tucson, Arizona, US, December, 2007.
- [84] Jens Schmitt, Frank Zdarsky, Lothar Thiele: **A Comprehensive Worst-Case Calculus for Wireless Sensor Networks with In-Network Processing.**
Real-Time Systems Symposium (RTSS 07), IEEE, Tucson, Arizona, US, December, 2007.
- [85] Wolfgang Haid, Lothar Thiele: **Complex Task Activation Schemes in System Level Performance Analysis.**
Proc. 5th Intl Conf. on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2007), ACM Press, Salzburg, Austria, pages 173-178, October, 2007.
- [86] Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: **Influence of Different System Abstractions on the Performance Analysis of Distributed Real-Time Systems.**
ACM & IEEE International Conference on Embedded Software (EMSOFT), ACM Press, Salzburg, Austria, pages 193-202, October, 2007.
- [87] Thomas Sporer, Andreas Franck, Iuliana Bacivarov, Michael Beckinger, Wolfgang Haid, Kai Huang, Lothar Thiele, Pier Paolucci, Piergiorgio Bazzana, Piero Vicini, Jianjiang Ceng, Stefan Kraemer, Rainer Leupers: **SHAPES - a Scalable Parallel HW/SW Architecture Applied to Wave Field Synthesis.**
Proc. 32nd Intl Audio Engineering Society (AES) Conference, Audio Engineering Society, Hillerod, Denmark, pages 175-187, September, 2007.
- [88] Lothar Thiele, Iuliana Bacivarov, Wolfgang Haid, Kai Huang: **Mapping Applications to Tiled Multiprocessor Embedded Systems.**
Proc. 7th Intl Conference on Application of Concurrency to System Design (ACSD 2007), IEEE Computer Society, Bratislava, Slovak Republic, pages 29-40, July, 2007.
- [89] Kai Huang, David Gruenert, Lothar Thiele: **Windowed FIFOs for FPGA-based Multiprocessor Systems.**
IEEE 18th International Conference on Application-specific Systems, Architectures and Processors(ASAP07), Montreal, Canada, pages 36-42, July, 2007.

- [90] Jan Beutel, Matthias Dyer, Roman Lim, Christian Plessl, Matthias Woehrle, Mustafa Yucecel, Lothar Thiele: **Automated Wireless Sensor Network Testing**. Proc. 4th Intl. Conf. Network Sensing Systems (INSS 2007), IEEE, pages 303, June, 2007.
- [91] Andreas Meier, Jan Beutel, Roman Lim, Lothar Thiele: **Design of a High-Reliability Low Power Status Monitoring Protocol**. Proc. 4th Intl. Conf. Networked Sensing Systems (INSS 2007), pages 2-9, June, 2007.
- [92] Matthias Woehrle, Christian Plessl, Jan Beutel, Lothar Thiele: **Increasing the Reliability of Wireless Sensor Networks with a Distributed Testing Framework**. Proc. 4th Workshop on Embedded Networked Sensors (EmNets 2007), ACM Press, New York, Cork, Ireland, pages 93-97, June, 2007.
- [93] Kai Huang, Lothar Thiele, Todor Stefanov, Ed Deprettere: **Performance Analysis of Multimedia Applications using Correlated Streams**. Design, Automation and Test in Europe (DATE 07), Nice, France, pages 912-917, April, 2007.
- [94] Matthias Dyer, Jan Beutel, Lothar Thiele: **S-XTC: A Signal-Strength Based Topology Control Algorithm for Sensor Networks**. Proc. 8th Intl. Symposium on Autonomous Decentralized Systems (ISADS 2007), IEEE CS Press, Los Alamitos, CA, pages 508-515, March, 2007.
- [95] Eckart Zitzler, Dimo Brockhoff, Lothar Thiele: **The Hypervolume Indicator Revisited: On the Design of Pareto-compliant Indicators Via Weighted Integration**. Proceedings of the 4th International Conference on Evolutionary Multi-Criterion Optimization (EMO 2007), Lecture Notes on Computer Science 4403, Springer-Verlag, Matsushima, Japan, Vol. 4403, pages 862-876, March, 2007.
- [96] Matthias Dyer, Jan Beutel, Lothar Thiele, Thomas Kalt, Patrice Oehen, Kevin Martin, Philipp Blum: **Deployment Support Network - A Toolkit for the Development of WSNs**. Proc. 4th European Conf. on Wireless Sensor Networks (EWSN 2007), Lecture Notes in Computer Science Vol. 4373, Springer, Berlin, pages 195-211, January, 2007.
- [97] Jan Beutel, Matthias Dyer, Mustafa Yucecel, Lothar Thiele: **Development and Test with the Deployment-Support Network**. Proc. 4th European Conf. on Wireless Sensor Networks (EWSN 2007), adjunct poster/demo proceedings, Parallel and Distributed Systems, TU Delft, The Netherlands, PDS-2007-001, pages 47-48, January, 2007.
- [98] Simon Künzli, Arne Hamann, Rolf Ernst, Lothar Thiele: **Combined Approach to System Level Performance Analysis of Embedded Systems**. International Conference on Hardware Software Codesign CODES/ISSS, Salzburg, Austria, pages 63 - 68, 2007.
- [99] Christian Plessl, Marco Platzner, Lothar Thiele: **Optimal Temporal Partitioning based on Slowdown and Retiming**. Proc. 5th Int. Conf. on Field Programmable Technology (FPT), IEEE Computer Society, pages 345-348, December, 2006.
- [100] Clemens Moser, Davide Brunelli, Lothar Thiele, Luca Benini: **Lazy Scheduling for Energy Harvesting Sensor Nodes**. From Model-Driven Design to Resource Management for Distributed Embedded Systems, IFIP International Federation for Information Processing, Springer, Boston, Vol. 225, pages 125-134, October, 2006.
- [101] Clemens Moser, Davide Brunelli, Lothar Thiele, Luca Benini: **Real-Time Scheduling with Regenerative Energy**.

- In Proceedings of the 18th Euromicro Conference on Real-Time Systems (ECRTS 06), Dresden, Germany, pages 261-270, July, 2006.
- [102] Ernesto Wandeler, Lothar Thiele: **Interface-Based Design of Real-Time Systems with Hierarchical Scheduling.**
12th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), San Jose, USA, pages 243-252, April, 2006.
- [103] Simon Künzli, Lothar Thiele: **Generating Event Traces Based on Arrival Curves.**
13th GI/ITG Conference on Measurement, Modeling, and Evaluation of Computer and Communication Systems (MMB), VDE Verlag, pages 81--98, March, 2006
- [104] Ernesto Wandeler, Alexandre Maxiaguine, Lothar Thiele: **Performance Analysis of Greedy Shapers in Real-Time Systems.**
Design, Automation and Test in Europe (DATE), Munich, Germany, pages 444-449, March, 2006.
- [105] Luca Negri, Lothar Thiele: **Power Management for Bluetooth Sensor Networks.**
Proc. 3rd European Workshop on Wireless Sensor Networks (EWSN 2006), Springer Verlag, Berlin, No. 3868, pages 196-211, February, 2006.
- [106] Ernesto Wandeler, Lothar Thiele: **Optimal TDMA Time Slot and Cycle Length Allocation.**
Asia and South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, pages 479-484, January, 2006.
- [107] Simon Künzli, Francesco Poletti, Luca Benini, Lothar Thiele: **Combining Simulation and Formal Methods for System-Level Performance Analysis.**
Design Automation and Test in Europe (DATE), IEEE Computer Society, pages 236-241, 2006.
- [108] Samarjit Chakraborty, Yanhong Liu, Nikolay Stoimenov, Lothar Thiele, Ernesto Wandeler: **Interface-Based Rate Analysis of Embedded Systems.**
7th IEEE International Real-Time Systems Symposium (RTSS 06), Rio de Janeiro, Brasil, pages 25-34, 2006.
- [109] Lothar Thiele, Ernesto Wandeler, Nikolay Stoimenov: **Real-time interfaces for composing real-time systems.**
International Conference On Embedded Software EMSOFT 06, Seoul, Korea, pages 34-43, 2006.
- [110] Pier Stanislao Paolucci, Lothar Thiele: **SHAPES: a tiled software hardware platform for embedded systems.**
Proceedings of the 4th international conference on Hardware/software codesign and system synthesis CODES/ISSS, ACM Press, Seoul, Korea, pages 167 - 172, 2006.
- [111] Lennart Meier, Philipp Blum, Lothar Thiele: **Interval-based Clock Synchronization Is Resilient To Mobility.**
Second IEEE International Conference on Mobile Ad Hoc and Sensor Systems (MASS 2005), Washington, DC, USA, pages 8-15, November, 2005.
- [112] Ernesto Wandeler, Joern Janneck, Edward Lee, Lothar Thiele: **Counting Interface Automata and their Application in Static Analysis of Actor Models.**
3rd International Conference on Software Engineering and Formal Methods - SEFM 2005, Koblenz, Germany, pages 106-116, September, 2005.
- [113] Alexandre Maxiaguine, Samarjit Chakraborty, Lothar Thiele: **DVS for Buffer-Constrained Architectures with Predictable QoS-Energy Tradeoffs.**

- CODES+ISSS 2005: Proceedings of the 3rd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis, ACM Press, Jersey City, NJ, USA, pages 111--116, September, 2005.
- [114] Ernesto Wandeler, Lothar Thiele: **Real-Time Interfaces for Interface-Based Design of Real-Time Systems with Fixed Priority Scheduling.**
ACM Conference on Embedded Software (EMSOFT), ACM Press, New York, USA, pages 80-89, September, 2005.
- [115] Lennart Meier, Lothar Thiele: **Gradient Clock Synchronization in Sensor Networks.**
Twenty-Fourth Annual ACM SIGACT-SIGOPS Symposium on Principles of Distributed Computing (PODC 2005), Las Vegas, Nevada, USA, pages 238-238, July, 2005.
- [116] Jan Beutel, Matthias Dyer, Lennart Meier, Lothar Thiele: **Scalable Topology Control for Deployment-Support Networks.**
Fourth International Symposium on Information Processing in Sensor Networks (IPSN 2005), ACM, pages 359-363, April, 2005.
- [117] Ernesto Wandeler, Lothar Thiele: **Characterizing Workload Correlations in Multi Processor Hard Real-Time Systems.**
11th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), IEEE, San Francisco, USA, pages 46--55, March, 2005.
- [118] Ernesto Wandeler, Lothar Thiele: **Abstracting Functionality for Modular Performance Analysis of Hard Real-Time Systems.**
Asia and South Pacific Design Automation Conference (ASP-DAC), Shanghai, P.R. China, pages 697--702, January, 2005.
- [119] Samarjit Chakraborty, Lothar Thiele: **A New Task Model for Streaming Applications and Its Schedulability Analysis.**
Proceedings DATE 2005, pages 486-491, 2005.
- [120] Lothar Thiele: **Modular Performance Analysis of Distributed Embedded Systems**
FORMATS 2005 -, Lecture Notes in Computer Science, Springer Verlag, Vol. 3829, pages 1-2, 2005.
- [121] Ernesto Wandeler, Lothar Thiele, Marcel Verhoef, Paul Lieveise: **System Architecture Evaluation Using Modular Performance Analysis - A Case Study.**
1st International Symposium on Leveraging Applications of Formal Methods (ISoLA), Paphos, Cyprus, October, 2004.
- [122] Philipp Blum, Lothar Thiele: **Trace-Based Evaluation of Clock-Synchronization Algorithms for Wireless Loudspeakers.**
Second Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia 2005), IEEE, Stockholm, Sweden, pages 7-12, September, 2004.
- [123] Simon Künzli, Stefan Bleuler, Lothar Thiele, Eckart Zitzler: **A Computer Engineering Benchmark Application for Multiobjective Optimizers.**
Applications of Multi-Objective Evolutionary Algorithms, World Scientific Publishing, pages 269-294, December, 2004.
- [124] Lennart Meier, Philipp Blum, Lothar Thiele: **Internal Synchronization of Drift-Constraint Clocks in Ad-Hoc Sensor Networks.**
Fifth ACM International Symposium on Mobile Ad Hoc Networking and Computing, Tokyo, Japan, pages 90-97, May, 2004.
- [125] Ernesto Wandeler, Alexander Maxiaguine, Lothar Thiele: **Quantitative Characterization of Event Streams in Analysis of Hard Real-Time Applications.**

- 10th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Toronto, Canada, pages 450—461, May, 2004.
- [126] Matthias Dyer, Marco Platzner, Lothar Thiele: **Efficient Execution of Process Networks on a Reconfigurable Hardware Virtual Machine.**
12th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa, CA, USA, April, 2004.
- [127] Philipp Blum, Lennart Meier, Lothar Thiele: **Improved Interval-Based Clock Synchronization in Sensor Networks.**
Third International Symposium on Information Processing in Sensor Networks, Berkeley, California, USA, pages 349-358, April, 2004.
- [128] Alexander Maxiaguine, Simon Künzli, Lothar Thiele: **Workload Characterization Model for Tasks with Variable Execution Demand.**
Design Automation and Test in Europe (DATE), IEEE Press, Paris, France, pages 1040-1045, February, 2004.
- [129] Jan Beutel, Oliver Kasten, Friedemann Mattern, Kay Roemer, Frank Siegemund, Lothar Thiele: **Prototyping Wireless Sensor Networks with BTnodes.**
1st European Workshop on Wireless Sensor Networks (EWSN 2004), Springer LNCS, Berlin, January, 2004.
- [130] Alexander Maxiaguine, Simon Künzli, Samarjit Chakraborty, Lothar Thiele: **Rate Analysis for Streaming Applications with On-chip Buffer Constraints.**
Asia South Pacific Design Automation Conference (ASP-DAC), Yokohama, Japan, pages 131-136, January, 2004.
- [131] Samarjit Chakraborty, Simon Künzli, Lothar Thiele: **A General Framework for Analysing System Properties in Platform-Based Embedded System Designs.**
Design Automation and Test in Europe (DATE), IEEE Press, Munich, Germany, pages 10190 --10195, March, 2003.
- [132] Christoph Steiger, Herbert Walder, Marco Platzner, Lothar Thiele: **Online Scheduling and Placement of Real-time Tasks to Partially Reconfigurable Devices.**
Proceedings of the 24th International Real-Time Systems Symposium (RTSS03), pages 224-235, 2003.
- [133] Eckart Zitzler, Marco Laumanns, Lothar Thiele: **SPEA2: Improving the Strength Pareto Evolutionary Algorithm for Multiobjective Optimization.**
Evolutionary Methods for Design, Optimisation, and Control, CIMNE, Barcelona, Spain, pages 95--100, 2002.
- [134] Lothar Thiele, Samarjit Chakraborty, Matthias Gries, Simon Künzli: **Design Space Exploration of Network Processor Architectures.**
First Workshop on Network Processors at the 8th International Symposium on High-Performance Computer Architecture (HPCA8), Cambridge MA, USA, pages 30-41, February, 2002.
- [135] Lothar Thiele, Samarjit Chakraborty, Matthias Gries, Simon Künzli: **A Framework for Evaluating Design Tradeoffs in Packet Processing Architectures.**
39th Design Automation Conference (DAC 2002), ACM Press, New Orleans LA, USA, pages 880-885, June, 2002.
- [136] Kalyanmoy Deb, Lothar Thiele, Marco Laumanns, Eckart Zitzler: **Scalable Multi-Objective Optimization Test Problems.**
Congress on Evolutionary Computation - CEC 2002, IEEE Press, Honolulu, HI, USA, pages 825--830, May, 2002.

- [137] Marco Laumanns, Lothar Thiele, Kalyanmoy Deb, Eckart Zitzler: **Archiving with Guaranteed Convergence And Diversity in Multi-objective Optimization.** GECCO 2002: Proceedings of the Genetic and Evolutionary Computation Conference, Morgan Kaufmann Publishers, New York, NY, USA, pages 439--447, July, 2002.
- [138] Eckart Zitzler, Marco Laumanns, Lothar Thiele, Carlos M. Fonseca, Viviane Grunert da Fonseca: **Why Quality Assessment Of Multiobjective Optimizers Is Difficult.** GECCO 2002: Proceedings of the Genetic and Evolutionary Computation Conference, Morgan Kaufmann Publishers, New York, NY, USA, pages 666-674, July, 2002.
- [139] Samarjit Chakraborty, Thomas Erlebach, Simon Künzli, Lothar Thiele: **Schedulability of Event-Driven Code Blocks in Real-Time Embedded Systems.** 39th Design Automation Conference (DAC 2002), ACM Press, New Orleans LA, USA, pages 616-621, June, 2002.
- [140] Marco Laumanns, Lothar Thiele, Eckart Zitzler, Emo Welzl, Kalyanmoy Deb: **Running time analysis of multi-objective evolutionary algorithms on a simple discrete optimization problem.** Parallel Problem Solving From Nature -- PPSN VII, Lecture Notes in Computer Science, Springer-Verlag, Granada, Spain, pages 44-53, September, 2002.
- [141] Philipp Blum, Lothar Thiele: **Clock Synchronization using Packet Streams.** Technical Report IRIT/2002-27-R, International Symposium on Distributed Computing, DISC 2002, Toulouse, France, pages 1-8, June, 2002.
- [142] Samarjit Chakraborty, Matthias Gries, Lothar Thiele: **Supporting a Low Delay Best-Effort Class in the Presence of Real-Time Traffic.** 8th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), IEEE Press, San Jose, California, pages 45-54, September, 2002.
- [143] Samarjit Chakraborty, Simon Künzli, Lothar Thiele: **Approximate Schedulability Analysis.** 23rd IEEE Real-Time Systems Symposium (RTSS), IEEE Press, Austin TX, USA, pages 159-168, December, 2002.
- [144] Christian Plessl, Rolf Enzler, Herbert Walder, Jan Beutel, Marco Platzner, Lothar Thiele: **Reconfigurable Hardware in Wearable Computing Nodes.** 6th International Symposium on Wearable Computers (ISWC2002), IEEE Computer Society, pages 215-222, Oktober, 2002.
- [145] Stefan Bleuler, Martin Brack, Lothar Thiele, Eckart Zitzler: **Multiobjective Genetic Programming: Reducing Bloat Using SPEA2.** Congress on Evolutionary Computation (CEC-2001), IEEE, pages 536--543, May, 2001.
- [146] Marco Laumanns, Eckart Zitzler, Lothar Thiele: **On The Effects of Archiving, Elitism, and Density Based Selection in Evolutionary Multi-Objective Optimization.** Evolutionary Multi-criterion Optimization (EMO 2001), Lecture Notes on Computer Science 1993, Springer, Zurich, Switzerland, pages 181-196, March, 2001.
- [147] Lothar Thiele, Samarjit Chakraborty, Matthias Gries, Alexander Maxiaguine, Jonas Greuter: **Embedded Software in Network Processors - Models and Algorithms.** Proceedings of the First Workshop on Embedded Software (EMSOFT), Lecture Notes in Computer Science 2211, Springer-Verlag, Lake Tahoe, California, USA, pages 416-434, Oktober, 2001.
- [148] Marco Laumanns, Eckart Zitzler, Lothar Thiele: **Multiple Criteria Decision Support by Evolutionary Computation.** Sustainability in the Information Society. 15th International Symposium Informatics for

Environmental Protection, Umwelt-Informatik aktuell, Metropolis Verlag, Zurich, Switzerland, pages 547-552, Oktober, 2001.

- [149] RolfENZler, Marco Platzner, Christian Plessl, Lothar Thiele, Gerhard Tröster: **Reconfigurable Processors for Handhelds and Wearables: Application Analysis.** Reconfigurable Technology: FPGAs and Reconfigurable Processors for Computing and Communications III (ITCom 2001), SPIE, Denver, Colorado, USA, Vol. 4525, pages 135-146, August, 2001.
- [150] Lothar Thiele: **Internal Design Representations for Embedded Systems.** Int. Conference on Computer Aided Design (ICCAD) 2001, IEEE, San Jose, 2001.
- [151] Samarjit Chakraborty, Thomas Erlebach, Lothar Thiele: **On the Complexity of Scheduling Conditional Real-Time Code.** Proceedings of the 7th International Workshop on Algorithms and Data Structures (WADS), Lecture Notes in Computer Science 2125, Springer-Verlag, Providence, Rhode Island, USA, pages 38--49, August, 2001.
- [152] Juergen Teich, Lothar Thiele: **Exact Partitioning of Affine Dependence Algorithms.** Lecture Notes in Computer Science, Vol. 2268, Springer, SAMOS - Systems, Architectures, Modeling and Simulation, pages 131-151, 2001.
- [153] Lothar Thiele, Samarjit Chakraborty, Martin Naedele: **Real-time Calculus for Scheduling Hard Real-Time Systems.** International Symposium on Circuits and Systems ISCAS 2000, Geneva, Switzerland, Vol. 4, pages 101-104, March, 2000.
- [154] Marco Laumanns, Eckart Zitzler, Lothar Thiele: **A Unified Model for Multi-Objective Evolutionary Algorithms with Elitism.** Congress on Evolutionary Computation (CEC-2000), IEEE, pages 46-53, July, 2000.
- [155] Dirk Ziegenbein, K Richter, Rolf Ernst, Juergen Teich, Karsten Strehl, Lothar Thiele, Marek Jerasek: **Embedded System Design Using SPI Workbench.** Proceeding of FDL 2000 (Forum on Design Languages), Tuebingen, Germany, September, 2000.
- [156] Karsten Strehl, Lothar Thiele, Dirk Ziegenbein, Rolf Ernst, Juergen Teich: **Scheduling Hardware/Software Systems Using Symbolic Techniques.** Proceedings of the 7th International Workshop on Hardware/Software Codesign (CODES '99), Rome, Italy, pages 173-177, May, 1999.
- [157] Karsten Strehl, Lothar Thiele: **Interval Diagram Techniques and Their Applications.** Proceedings of the 8th International Workshop on Post-Binary ULSI Systems, Freiburg im Breisgau, Germany, pages 23-24, May, 1999.
- [158] Matthias Anlauff, Philipp W. Kutter, Alfonso Pierantonio, Lothar Thiele: **Generating an Action Notation Environment from Montages Descriptions.** Proceedings of the Second International Workshop on Action Semantics, BRICS Notes Series, NS-99-3, Amsterdam, The Netherland, pages 1-41, March, 1999.
- [159] Martin Naedele, Lothar Thiele, Michael Eisenring: **Characterising Variable Task Releases and Processor Capacities.** 14th IFAC World Congress 1999, Beijing, July, 1999.
- [160] K Richter, Dirk Ziegenbein, Rolf Ernst, Lothar Thiele, Juergen Teich: **Representation of Function Variants for Embedded System Optimization and Synthesis.** Proceedings of 36th Design Automation Conference, pages 517-523, January, 1999.

- [161] Karsten Strehl, Lothar Thiele: **Interval Diagram Techniques for Symbolic Model Checking of Petri Nets.**
Proceedings of the Design, Automation and Test in Europe Conference (DATE99), Munich, Germany, pages 756-757, March, 1999.
- [162] Lothar Thiele, Karsten Strehl, Dirk Ziegenbein, Rolf Ernst, Juergen Teich: **FunState - An Internal Design Representation for Codesign.**
Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD-99), San Jose, California, pages 558-565, November, 1999.
- [163] Rolf Ernst, Dirk Ziegenbein, K Richter, Lothar Thiele, Juergen Teich: **Hardware/Software Codesign of Embedded Systems.**
Proceedings IEEE Workshop on VLSI, Orlando, U.S.A., June, 1999.
- [164] Dirk Ziegenbein, K Richter, Rolf Ernst, Lothar Thiele, Juergen Teich: **An Internal Representation for Heterogeneously Specified Embedded Systems.**
Proceedings GI/ITG/GMM Workshop on Design Methods and Specification Languages, Braunschweig, Germany, February, 1999.
- [165] Michael Eisenring, Marco Platzner, Lothar Thiele: **Communication Synthesis for Reconfigurable Embedded Systems.**
9th International Workshop on Field-Programmable Logic and Applications, FPL 99, Lecture Notes in Computer Science, 1673, pages 205-214, August, 1999.
- [166] Eckart Zitzler, Kalyanmoy Deb, Lothar Thiele: **Comparison of Multiobjective Evolutionary Algorithms on Test Functions of Different Difficulty.**
Genetic and Evolutionary Computation Conference (GECCO-99): Bird-of-a-feather Workshop on Multi-criterion Optimization, Orlando, USA, pages 121-122, July, 1999.
- [167] Michael Eisenring, Juergen Teich, Lothar Thiele: **Rapid Prototyping of Dataflow Programs on Hardware/Software Architectures.**
Proc. of HICSS-31, Proc. of the Hawai Int. Conf. on System Sciences, Vol. 3, pages 187-196, January, 1998.
- [168] Eckart Zitzler, Lothar Thiele: **Multiobjective Optimization Using Evolutionary Algorithms - A Comparative Case Study.**
PPSN-V, Amsterdam, pages 292-301, September, 1998.
- [169] Philipp W. Kutter, Daniel Schweizer, Lothar Thiele: **Integrating Domain Specific Language Design in the Software Life Cycle.**
Proceedings of Current Trends in Applied Formal Methods, Boppard, Germany, Oktober, 1998.
- [170] Karsten Strehl, Lothar Thiele: **Symbolic Model Checking of Process Networks Using Interval Diagram Techniques.**
Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD-98), San Jose, California, pages 686-692, November, 1998.
- [171] Dirk Ziegenbein, Rolf Ernst, K Richter, Juergen Teich, Lothar Thiele: **Combining Multiple Models of Computation for Scheduling and Allocation.**
Proceedings 6th International Workshop on Hardware/Software Codesign (Codes/Cashe 98), Seattle, U.S.A., pages 9-13, March, 1998.
- [172] Dirk Ziegenbein, Rolf Ernst, Juergen Teich, Lothar Thiele: **Representation of Process Mode Correlation for Scheduling.**
Proceedings International Conference on Computer-Aided Design (ICCAD 98), San Jose, U.S.A., pages 54 -61, March, 1998.

- [173] Uwe Schwiegelshohn, Lothar Thiele: **Some properties of change diagrams.**
A. Yakovlev and L. Gomes, editors, Proceedings of the 19th International Conference on Application and Theory of Petri Nets, pages 12-25, July, 1998.
- [174] Michael Eisenring, Juergen Teich, Lothar Thiele: **Domain-Specific Interface Generation from Dataflow Specifications.**
Codes/CASHE 98, Seattle, Washington, pages 43-47, March, 1998.
- [175] Juergen Teich, Tobias Blickle, Lothar Thiele: **An Evolutionary Approach to System-Level Synthesis.**
In Proc. of Codes/CASHE 97 - the 5th Int. Workshop on Hardware/Software Codesign, Braunschweig, Germany, pages 167-171, March, 1997.
- [176] Uwe Schwiegelshohn, Lothar Thiele: **Periodic and non-periodic min-max equation.**
In Degano, P., Gorrieri, R., and Marchetti-Spaccamela, A., editors, ICALP 97: 24th International Colloquium on Automata, Languages, and Programming, c, Bologna, Italy, pages 379-389, January, 1997.
- [177] Lothar Thiele, Jose Fortes, Kees Vissers, Valerie Taylor, Tobias Noll, Juergen Teich: **Proc. IEEE Int. Conf. on Application Specific Systems, Architectures, and Processors.**
IEEE Computer Society Press, Los Alamitos, CA, July, 1997.
- [178] Tobias Blickle, Juergen Teich, Lothar Thiele: **An Evolutionary Approach to System-Level Synthesis.**
WSC1, the 1st Online Workshop on Soft Computing, Nagoya, Japan, pages 251-256, August, 1996.
- [179] Matthias Schoebinger, Lothar Thiele: **Synthesis of Domain-Specific Heterogeneous Multiprocessor Systems.**
IEEE Symposium on Circuits and Systems, Atlanta, Georgia, January, 1996.
- [180] Juergen Teich, Tobias Blickle, Lothar Thiele: **An evolutionary approach to system-synthesis.**
In Furuhashi, T. editor, Proceedings of the First Online Workshop on Soft Computing, pages 251-256, January, 1996.
- [181] Juergen Teich, Lothar Thiele, Lee Zhang: **Scheduling of partitioned regular algorithms on processor arrays with constrained resources.**
In Proc. Int. Conf. on Application-Specific Systems, Architectures, and Processors (ASAP96), Chicago, U.S.A., pages 131-144, August, 1996.
- [182] Jean-Paul Theis, Lothar Thiele: **VLIW-Processors under Periodic Real Time Constraints.**
IEEE Intl. Conf. on Computer Design 1996, Austin, Texas, January, 1996. Tobias Blickle, Lothar Thiele: **A Mathematical Analysis of Tournament Selection..**
Proceedings of the Sixth International Conference on Genetic Algorithms, San Francisco, CA., pages 9-16, January, 1995.
- [183] Juergen Teich, Lothar Thiele, Edward Lee: **Modeling and Simulation of Heterogeneous Real-Time Systems Based on a Deterministic Discrete Event Model.**
Proc. 8th Int. Symp. on System Synthesis, Cannes, France, pages 156-16, September, 1995.
- [184] Jean-Paul Theis, Lothar Thiele: **POM-A processor model for image processing.**
In Proc. IEEE. Int. Conf. on Computer Design, IEEE Computer Society Press, Austin, Texas, Oktober, 1995.

- [185] Ulrich Arzt, Lothar Thiele: **Hierarchical specification of algorithms and VLSI-architectures.**
Int. Workshop on VLSI Signal Processing, La Jolla, U.S.A., January, 1994.
- [186] Tobias Blickle, Joachim König-Baltes, Lothar Thiele: **A Prototyping Array for Parallel Architectures.**
W.R. Moore and W.Luk, editors, FPGAs, Abingdon EE/CS Books, England, pages 388-397, January, 1994.
- [187] Joachim König-Baltes, Lothar Thiele: **A High Speed FPGA-Based Interface to High Bandwidth Hardware.**
W.R. Moore and W.Luk, editors, FPGAs, pages 345-352, January, 1994.
- [188] Claudia Riem, Joachim König-Baltes, Lothar Thiele: **A Case Study in Algorithm--Architecture Codesign: Hardware Accelerator for Long Integer Arithmetic.**
Algorithms and Parallel VLSI Architectures III, Elsevier Publ., pages 119-130, January, 1994.
- [189] Claudia Riem, Joachim König-Baltes, Lothar Thiele: **Eine Fallstudie zum Algorithmus--Architektur Codesign: Koprozessor für Arithmetik auf langen Zahlen.**
Abstracts des GI/ITG-Workshops Architektuern für hochintegrierte Schaltungen, Schloss Dagstuhl, Germany, January, 1994.
- [190] Claudia Riem, Joachim König-Baltes, Lothar Thiele: **A case study in Algorithm-ARchitecture Codesign: Hardware Accelerator for Long Integer Arithmetic.**
3rd International Workshop on Algorithms and Parallel VLSI Architectures, Katholieke Universiteit Leuven, Belgium, January, 1994.
- [191] Juergen Teich, Shruva Sriram, Lothar Thiele, M Martin: **Performance analysis of mixed asynchronous-synchronous systems.**
IEEE Int. Workshop on VLSI Signal Processing 94, La Jolla, USA, pages 103-112, Oktober, 1994.
- [192] Tobias Blickle, Lothar Thiele: **Genetic programming and redundancy..**
Genetic Algorithms within the Framework of Evolutionary Computation (Workshop at KI-94), Saarbrücken, pages 33-38, January, 1994.
- [193] Tobias Blickle, Joachim König-Baltes, Lothar Thiele: **A Prototyping Array for Parallel Architectures.**
3rd International Workshop on Field Programmable Logic and Applications, Jesus College, University of Oxford, England, January, 1993.
- [194] A Bachmann, Matthias Schoebinger, Lothar Thiele: **Synthesis of domain specific multiprocessor systems including memory design.**
VLSI Signal Processing VI, IEEE Press, New York, pages 417-425, January, 1993.
- [195] Christian Heckler, Lothar Thiele: **Parallel complexity of lattice basis reduction and a floating-point parallel algorithm.**
PARLE93, Springer-Verlag, Munich, pages 744-747, January, 1993.
- [196] Christian Heckler, Lothar Thiele: **A parallel lattice basis reduction for mesh-connected processor arrays and parallel complexity.**
SPDP 93, Dallas, pages 400-407, January, 1993.
- [197] Joachim König-Baltes, Lothar Thiele: **A High Speed FPGA-Based Interface to High Bandwidth Hardware.**
In Proc 3rd International Workshop on Field Programmable Logic and Applications, Jesus College, University of Oxford, England, January, 1993.

- [198] Juergen Teich, Lee Zhang, Lothar Thiele: **Minimal communication in massively parallel architectures.**
PARS Workshop 93, Dresden, Germany, pages 154-161, April, 1993.
- [199] Lothar Thiele: **Design methods for algorithmically specified processor arrays.**
In Proc. of PARS Workshop 93, Dresden, Germany, pages 141-153, April, 1993.
- [200] Lothar Thiele: **Resource constraint scheduling of uniform algorithms..**
Conf. on Application Specific Processor Arrays, Venice, Italy, pages 29-40, Oktober, 1993.
- [201] Ulrich Arzt, Daniela Merziger, Lothar Thiele: **Rekursive Prozeduraufrufe in VLSI-Occam.**
Parallele Datenverarbeitung mit dem Transputer, Informatik Fachberichte, Springer Verlag, Berlin, Heidelberg, pages 108-115, January, 1992.
- [202] Ulrich Arzt, Juergen Teich, Lothar Thiele: **The concepts of COMPAR: A compiler for massive parallel architectures.**
International Symposium on Circuits and Systems (ISCAS), San Diego, pages 681-684, May, 1992.
- [203] Ulrich Arzt, Juergen Teich, Lothar Thiele: **Hierarchical concepts in the design of processor arrays.**
CompEuro 1992, The Hague, pages 232-238, May, 1992.
- [204] Wolfgang Backes, Uwe Schwiegelshohn, Lothar Thiele: **Analysis of free schedule in periodic graphs.**
4th Annual ACM Symposium on Parallel Algorithms and Architectures, San Diego, USA, pages 333-342, June, 1992.
- [205] Gerhard Fettweis, Lothar Thiele: **Algebraic recurrence transformations for massive parallelism.**
VLSI Signal Processing, IEEE Press, pages 332-341. IEEE Press, Oktober, 1992.
- [206] Juergen Teich, Lothar Thiele: **A transformative approach to the partitioning of processor arrays..**
In Proc. Int. Conf. on Application Specific Array Processors, IEEE Computer Society Press, Berkeley, pages 4-20, August, 1992.
- [207] Lothar Thiele: **Design methods for parallel signal processing architectures..**
ProRisc Workshop on Architectures and Algorithms for Signal Processing, Houthalen, Belgium, April, 1992.
- [208] Juergen Teich, Lothar Thiele: **Control generation in the design of processor arrays.**
Kluwer Academic Publishers, January, 1992.
- [209] Lothar Thiele: **Compiler techniques for massive parallel architectures..**
Kluwer Academic Publishers, January, 1992.
- [210] Ulrich Arzt, Daniela Merziger, Lothar Thiele: **Preprozessor zum Auflösen rekursiver Prozeduraufrufe in VLSI-Occam.**
Transputer Anwender Treffen (TAT), Aachen, pages 60-61, July, 1991.
- [211] Ulrich Arzt, Lothar Thiele: **VLSI-Occam.**
GME/GI-Fachtagung Mikroelektronik, Baden-Baden, pages 229-235, January, 1991.
- [212] Ulrich Arzt, Lothar Thiele: **Hardware description with VLSI-Occam.**
IFIP 10th International Computer Hardware Description Languages, Marseille, April, 1991.
- [213] Wolfgang Backes, Uwe Schwiegelshohn, Lothar Thiele: **Optimal scheduling of loop programs and multidimensional discrete event systems.**

- Int. Symp. Mathematical Theory of Networks and Systems MTNS 91, Kobe, Japan, June, 1991.
- [214] Juergen Teich, Lothar Thiele: **Uniform design of parallel programs for DSP..**
IEEE Int. Symp. Circuits and Systems, Singapore, pages 344a-347a, June, 1991.
- [215] Ulrich Arzt, Lothar Thiele: **Simulation von VLSI-Schaltungen auf dem Transputer.**
Transputer Anwender Treffen (TAT), Aachen, pages 165-170, January, 1990.
- [216] Jichun Bu, Lothar Thiele, Ed Deprettere: **Systolic array implementation of nested loop programs.**
In Application Specific Array Processors, IEEE Computer Society Press, Princeton, pages 31-43, September, 1990.
- [217] Gerhard Fettweis, Lothar Thiele, Heinrich Meyr: **Algorithm transformations for unlimited parallelism.**
IEEE Int. Symp. Circuits and Systems, New Orleans, pages 1756-1759, May, 1990.
- [218] Karl Huber, Juergen Teich, Lothar Thiele: **Design of configurable processor arrays (invited paper).**
In Proc. IEEE Int. Symp. Circuits and Systems, New Orleans, pages 970-973, May, 1990.
- [219] Lothar Thiele, Vwani Roychowdhury: **Optimal solution to the affine communication problem.**
Int. Workshop on Algorithms and Parallel VLSI Architectures, Pont-a-Mousson, France, pages 122-126, June, 1990.
- [220] Lothar Thiele, Vwani Roychowdhury: **Systematic design of local processor arrays for numerical algorithms.**
Parallel Algorithms and VLSI Architectures: Volume A (E. Deprettere Ed.), North Holland Publishers, pages 329-339, January, 1990.
- [221] Vwani Roychowdhury, Lothar Thiele, Sailesh Rao, Thomas Kailath: **On the localization of algorithms for VLSI processor arrays.**
VLSI Signal Processing III, IEEE Press, New York, pages 459-470, January, 1989.
- [222] Lothar Thiele: **Design of local concurrent algorithms (invited paper).**
Int. Symp. Mathematical Theory of Networks and Systems MTNS 89, Amsterdam, pages 102, January, 1989.
- [223] Lothar Thiele: **From linear recursions to computing arrays.**
IEEE Conf. on Circuits and Systems, Nanjing, China, pages 115-118, January, 1989.
- [224] Lothar Thiele: **On the design of piecewise regular processor arrays.**
IEEE Symp. on Circuits and Systems, Portland, pages 2239-2242, January, 1989.
- [225] Lothar Thiele: **VLSI processor arrays.**
GME/GI-Fachbericht 4, Mikroelektronik, VDE-Verlag Berlin, pages 77-84, January, 1989.
- [226] P Bergmann, Wolfgang Paul, Lothar Thiele: **Implementation of an information theoretic approach to computer vision.**
Workshop on Dynamic Networks, Eisenach, January, 1988.
- [227] P Bergmann, Wolfgang Paul, Lothar Thiele: **Implementierung eines informationstheoretischen Ansatzes zur Bilderkennung.**
Innovative Informations Infrastrukturen, Informatik Fachberichte 184, Springer-Verlag, Berlin, pages 187-197, January, 1988.

- [228] Vwani Roychowdhury, Lothar Thiele, Sailesh Rao, Thomas Kailath: **Design of local VLSI processor arrays.**
Int. Conf. on VLSI and Signal Processing, Monterey, November, 1988.
- [229] Lothar Thiele: **Computational arrays for Jacobi algorithms.**
SVD and Signal Processing, North Holland, pages 369-383, January, 1988.
- [230] Lothar Thiele: **On the hierarchical design of VLSI processor arrays.**
IEEE Symp. on Circuits and Systems, Helsinki, pages 2517-2520, January, 1988.
- [231] Lothar Thiele: **On the optimization of regular wavefront arrays.**
IEEE Conf. on Acoust., Speech, and Signal Processing, New York, pages 2029-2032, January, 1988.
- [232] Uwe Schwiegelshohn, Lothar Thiele: **A systolic array for the assignment problem.**
COMPEURO 87, Hamburg, pages 888-889, May, 1987.
- [233] Uwe Schwiegelshohn, Lothar Thiele: **One- and two-dimensional arrays for least squares problems.**
Acoust. Speech Signal Processing, Dallas, pages 791-794, January, 1987.
- [234] Uwe Schwiegelshohn, Lothar Thiele: **On the systolic computation of shortest paths.**
Parallel Processing, Charles, Illinois, pages 762-764, August, 1986.
- [235] Lothar Thiele: **Balanced model reduction in time and frequency domain.**
Int. Symp. Circuits and Systems, Kyoto, pages 345-348, January, 1985.
- [236] Lothar Thiele: **Applications of weighting functions in the analysis and synthesis of state-space systems.**
Fifth Symp. on Network Theory, Srajevo, pages 91-96, January, 1984.
- [237] Lothar Thiele: **Generalized Gramian matrices and their applications in digital filters.**
Digital Signal Processing-84, Elsevier Science Publishers, North Holland, pages 13-17, January, 1984.
- [238] Vedat Tavsanoglu, Lothar Thiele: **Simultaneous minimization of round-off noise and sensitivity in state-space digital filters.**
IEEE Int. Symp. Circuits and Systems, New Port Beach, pages 815-818, January, 1983.
- [239] Lothar Thiele: **On the realization of minimum sensitivity and minimum round-off noise state-space discrete systems.**
In Proc. Europ. Conf. Circuit Theory and Design, pages 151-153, January, 1983.

Books and Varia

- [240] Lothar Thiele: **Analytische Netzwerksynthese.**
Oldenbourg Verlag, Munchen, January, 1986.
- [241] Lothar Thiele: **Algorithmisch spezialisierte Strukturen für integrierte Schaltungen.**
Habilitation Thesis, Technische Universität München, January, 1986.
- [242] Lothar Thiele: **Zur Approximation und Realisierung elektrischer Netzwerke mit den Methoden der linearen Algebra.**
Technische Universität München, PhD Thesis, January, 1985.

- [243] Lothar Thiele, Jose Fortes, Kees Vissers, Valerie Taylor, Juergen Teich: **Application Specific Systems, Architectures and Processors.**
IEEE Computer Society Press, August, 1997.
- [244] Kalyanmoy Deb, Lothar Thiele, Eckart Zitzler: **First International Conference on Evolutionary Multi-Criterion Optimization (EMO) 2001.**
Lecture Notes on Computer Science 1993, Springer Verlag, ETH Zurich, Switzerland, March, 2001.
- [245] Yuri Gurevich, Philipp W. Kutter, Martin Odersky, Lothar Thiele: **International Workshop on Abstract State Machines, Theory and Applications (ASM 2000).**
Lecture Notes in Computer Science 1912, Springer-Verlag, Monte Verita, Switzerland,, March, 2000.
- [246] Fonseca, C.M., Fleming, P.J., Zitzler, E., Deb, K., Thiele, L.: **Evolutionary Multi-Criterion Optimization (EMO) 2003.**
Lecture Notes on Computer Science 2632, Springer Verlag, March, 2003.
- [247] Lothar Thiele, Manfred Morari: **Hybrid Systems: Computation and Control.**
Springer Verlag, March, 2005.
- [248] Jonas Greutert, Lothar Thiele: **RNOS - A Middleware Platform for Low-Cost Packet-Processing Devices.**
Network Processor Design, Issues and Practices Vol. 3, Morgan-Kaufmann, pages 173--195, 2005.
- [249] Lothar Thiele, Ernesto Wandeler: **Performance Analysis of Embedded Systems**
Handbook of Embedded Systems, Richard Zurawski ed., CRC Press, 2005.
- [250] Simon Künzli, Lothar Thiele, Eckart Zitzler: **Multi-criteria Decision Making in Embedded System Design.**
System-on-Chip: Next Generation Electronics, Al-Hashimi, B. M., Eds., IEE Press, pages 3-28, 2006.
- [251] Paul Lukowicz, Lothar Thiele, Gerhard Tröster: **Architecture of Computing Systems.**
Springer, Zurich, Switzerland, ARCS 2007: 20th International Conference, March 12-17, 2007.
- [252] Matthias Woehrle, Jan Beutel, Lothar Thiele: **Wireless Sensor Networks Test and Validation.**
CRC Press/Taylor & Francis, Chapter in Handbook of Networked Embedded Systems, 2009.
- [253] Lothar Thiele, Ernesto Wandeler, Wolfgang Haid: **Performance Analysis of Distributed Embedded Systems.**
Networked Embedded Systems Handbook, CRC Press/Taylor & Francis, 2009.
- [254] Lothar Thiele, Simon Perathoner: **Performance Prediction of Distributed Platforms**
Model-Based Design of Heterogeneous Embedded Systems, CRC Press, 2009.

Lothar Thiele

Swiss Federal Institute of Technology (ETH) Zurich
Computer Engineering and Networks Laboratory
CH-8092 Zurich
ph: +41 44 632 7031 fax: +41 44 632 1035
email: thiele@tik.ee.ethz.ch

Professional Experience

1981 - 1986 Technical University Munich Munich, Germany
Research Assistant

- Student education in Network Theory
- Research projects in Network Theory and Computing
- Software and Hardware Design

1987 Stanford University Stanford, CA
Research Associate

- Member of Information Systems Lab., Prof. T. Kailath
- Research in Computing

1988-1994 University Saarland Saarbrücken, Germany
Full Professor

- Education in Microelectronics
- Dean of Electrical Engineering Department
- Leading numerous research projects, funded by various companies and research foundations
- Research in microelectronics and computer engineering

1990 NEC C&C Laboratories Tokyo, Japan
Leave of absence

- Parallel and distributed computing at the Computer and Communications Lab, Kawasaki

1991 IBM Research Yorktown Heights, NY
Leave of absence

- Software and hardware development at the T.J. Watson Research Center

from 1994 ETH Zurich Zurich, Switzerland
Full Professor

- Education in Computer Engineering
- Leading the Computer Engineering and Networks Lab (about 80 people)
- Leading numerous research projects, funded by various companies and research foundations such as KT1, EU FP6, EU FP7, SNF
- Contracts and research projects with national and international companies such as HP, ESEC, NetEngines, InAlp, IBM, BridgeCo, Siemens
- Research in the areas of computer engineering, embedded systems, wearable and mobile computing systems, bio-inspired optimization methods
- Involved in large national and international research projects, such as ARTIST2 European Network of Excellence, SHAPES European

Integrated Project in FP 6, PREDATOR (FP7), COMBEST (FP7), Pro3D (FP7), EURETILE (FP7), MICS Mobile Information and Communication National Research Program

Education

- 1999 Hewlett-Packard Palo Alto, CA
Leave of absence
- Software and hardware design at the HP Research Labs
- 1963-1976 Various schools Aachen, Germany
- School education, final degree with distinction (best of year)
- 1976 Jury Superieur de Belgique Brussels, Belgium
- Final concert exam in piano (with grande distinction)
- 1976-1978 RWTH Aachen Aachen, Germany
- Studies in Electrical Engineering at the Technical University in Aachen
- 1971-1981 Technical University Munich, Germany
- Master in Electrical Engineering (with distinction, best of year)
- 1981-1984 Technical University Munich, Germany
- PhD (with distinction)
- 1984-1987 Technical University Munich, Germany
- Habilitation Thesis (venia legendi)

Major Awards

- 1977
- Studienstiftung des Deutschen Volkes
- 1986
- Award for the best PhD thesis
- 1987
- Outstanding Young Author Award of the IEEE
- 1988
- 1988 Browder J. Thompson Memorial Prize Award of the IEEE
- 2000
- IBM Faculty Achievement Award
- 2001
- IBM Faculty Achievement Award
- 2004
- Member of German Academy of Sciences Leopoldina

2005

- Recipient of the Honorary Blaise Pascal Chair of the University Leiden, The Netherlands

Varia

Professional Services

- Organization of several international conferences, member of steering boards (EMSOFT, FORMATS), member of program committees in major conferences, general chair of several conferences and workshops.
- Regular reviewing of large international research projects in various areas.
- Editorial board of several scientific journals such as VLSI Signal Processing, INTEGRATION, IEEE Trans. on Evolutionary Computation, IEEE Trans. on Industrial Informatics.
- Member of several scientific organizations such as IEEE and ACM, partly with organizational duties such as chairing ACM SIGBED (special interest group on embedded systems).
- Head of evaluation committees of various Information Technology and Electrical Engineering departments in Germany.
- Various institutional services within the ETH Zurich, such as representing ETH Zurich in affairs related to Bologna treaty, leading evaluation committees, study director of Information Technology and Electrical Engineering department (D-ITET), member of Hochschulversammlung, member of research commission of ETH Zurich, member of planning commission of ETH Zurich, Vice-president of KdL.
- Member of Steering Committee of the ALARI Master of Embedded System Program at University Lugano.
- Member of Advisory Board of ESI (Embedded System Institute, Eindhoven).
- Member of the Foundation Board of Hasler Foundation, Switzerland.

Research Interests

- Optimization, bio-inspired techniques for multi-objective problems
- Models, methods and software tools for the design of embedded systems
- Design of mobile information and communication systems, including wearable computing and sensor networks
- Further information about research and education:
<http://www.tik.ee.ethz.ch/~thiele/>

Private Data

- Date and place of birth: 7th of April 1957, Aachen, Germany
- Three children (1986, 1989, 1993)
- Married since 1982

Private Address

Lothar Thiele
Gladbachstrasse 89
CH-8044 Zurich